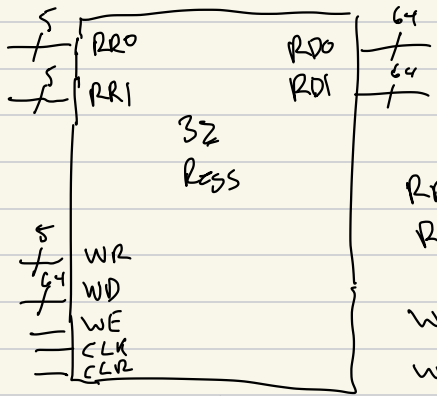
CS 631-01 Processor Design 2026-04-14

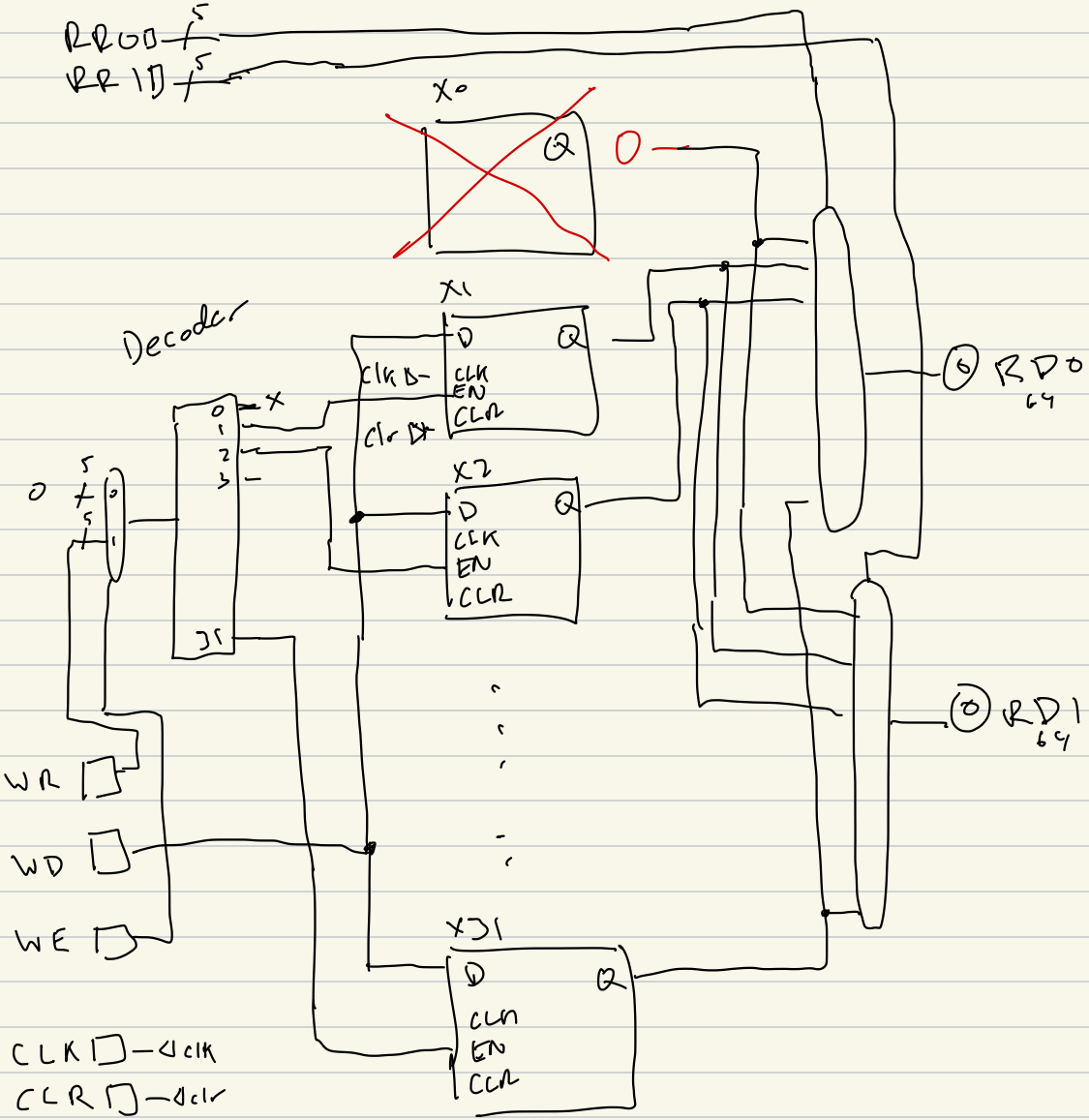
Register file



RR - read reg #
RD - read data value

WR - write register
WD - write data
WE - write enable

on a single clock cycle:
1) read up to two reg values
2) write at most to one register


RR0
5
RR1
5
X0
Q
0
X1
D
Q
CLK
EN
CLR
Decoder
0
1
2
3
X
X2
D
Q
CLK
EN
CLR
0
5
5
0
1
RD0
64
RD1
64
WR
WD
WE
XJ1
D
Q
CLK
EN
CLR
CLK
CLR

ALU Arithmetic Logic Unit